Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4019	438/595.ccls. 438/638.ccls. 438/639.ccls. 438/640.ccls. 438/672.ccls. 438/675.ccls. 257/775.ccls.	US-PGPUB; USPAT	OR	OFF	2005/04/05 09:18
L2	120	(438/595.ccls. 438/638.ccls. 438/639.ccls. 438/640.ccls. 438/672.ccls. 438/675.ccls. 257/775.ccls.) and ((gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) same (hole opening via trench groove window) same (contact plug stud land$6 pad) same (taper$6 funnel conical cone (isotropic$8 with etch$6)))	US-PGPUB; USPAT	OR	ON	2005/04/05 10:59
L3	91	(438/595.ccls. 438/638.ccls. 438/639.ccls. 438/640.ccls. 438/672.ccls. 438/675.ccls. 257/775.ccls.) and (((hole opening via trench groove window) with (liner spacer sidewall (side adj wall))) same (contact plug stud land$6 pad) same (taper$6 funnel conical cone))	US-PGPUB; USPAT	OR	ON	2005/04/05 09:44
L4	121	((gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) same ((hole opening via trench groove window) with (liner spacer sidewall (side adj wall))) same (contact plug stud land$6 pad) same (taper$6 funnel conical cone)) and (semiconductor wafer silicon substrate)	US-PGPUB; USPAT	OR	ON	2005/04/05 09:52
L5	208	(gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) and (hole opening via trench groove window) and (contact plug stud land$6 pad) and (taper$6 funnel conical cone) and (semiconductor wafer silicon substrate)	EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/05 11:06
L6	215	((hole opening via trench groove window) with (liner spacer sidewall (side adj wall))) and (contact plug stud land$6 pad) and (taper$6 funnel conical cone) and (semiconductor wafer silicon substrate)	EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/05 10:08

L7	348	((gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) same ((hole opening via trench groove window) with (taper$6 funnel conical cone)) same (contact plug stud land$6 pad)) and (semiconductor wafer silicon substrate)	US-PGPUB; USPAT	OR	ON	2005/04/05 11:13
L8	677	(438/595.ccls. 438/638.ccls. 438/639.ccls. 438/640.ccls. 438/672.ccls. 438/675.ccls. 257/775.ccls.) and ((gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) same (hole opening via trench groove window) same (contact plug stud land$6 pad) same (liner spacer sidewall (side adj wall)))	US-PGPUB; USPAT	OR	ON	2005/04/05 11:04
L9	131	(438/595.ccls. 438/638.ccls. 438/639.ccls. 438/640.ccls. 438/672.ccls. 438/675.ccls. 257/775.ccls.) and ((gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) same (hole opening via trench groove window) same (contact plug stud land$6 pad) same (liner barrier adhesion) same (spacer sidewall (side adj wall)))	US-PGPUB; USPAT	OR	ON	2005/04/05 11:17
L10	1156	(438/595.ccls. 438/638.ccls. 438/639.ccls. 438/640.ccls. 438/672.ccls. 438/675.ccls. 257/775.ccls.) and ((gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) same (hole opening via trench groove window contact plug stud land$6 pad) same (liner spacer sidewall (side adj wall)))	US-PGPUB; USPAT	OR	ON	2005/04/05 15:37
L11	4547	(gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) and (hole opening via trench groove window) and (contact plug stud land$6 pad) and (liner spacer sidewall (side adj wall)) and (semiconductor wafer silicon substrate)	EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/05 11:08

L12	3340	(gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) same (hole opening via trench groove window) same (contact plug stud land$6 pad) same (liner spacer sidewall (side adj wall))	EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/05 11:07
L13	1666	(gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) same ((hole opening via trench groove window) with (contact plug stud land$6 pad) with (liner spacer sidewall (side adj wall)))	EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/05 11:08
L14	505	(gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) and (hole opening via trench groove window) and (contact plug stud land$6 pad) and (liner barrier adhesion) and (spacer sidewall (side adj wall)) and (semiconductor wafer silicon substrate)	EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/05 11:09
L15	180	((gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) with (spacer sidewall (side adj wall))) and ((hole opening via trench groove window) with (liner barrier adhesion)) and (contact plug stud land$6 pad)	EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/05 12:22
L16	442	((gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) with (spacer sidewall (side adj wall))) same ((hole opening via trench groove window) with (liner barrier adhesion)) same (contact plug stud land$6 pad)	US-PGPUB; USPAT	OR	ON	2005/04/05 11:15
L17	434	16 and (semiconductor wafer silicon substrate)	US-PGPUB; USPAT	OR	ON	2005/04/05 11:14
L18	438	16 not 7	US-PGPUB; USPAT	OR	ON	2005/04/05 11:14
L19	355	((gate wordline bitline ((word bit metal coduct$6) adj (line trace runner interconnect$6))) with (spacer sidewall (side adj wall))) same ((hole opening via trench groove window) with (liner barrier adhesion) with (contact plug stud land$6 pad))	US-PGPUB; USPAT	OR	ON	2005/04/05 14:30